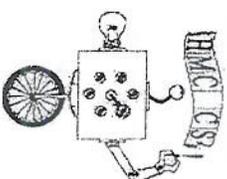


NAME _____

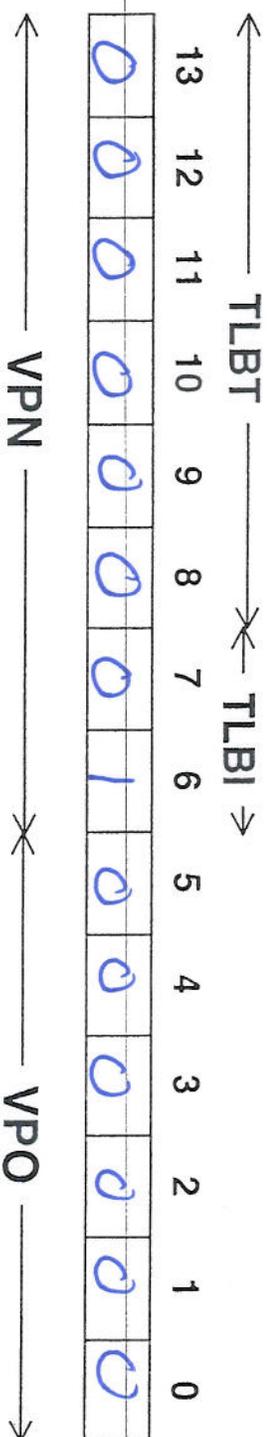
Q8



Address Translation

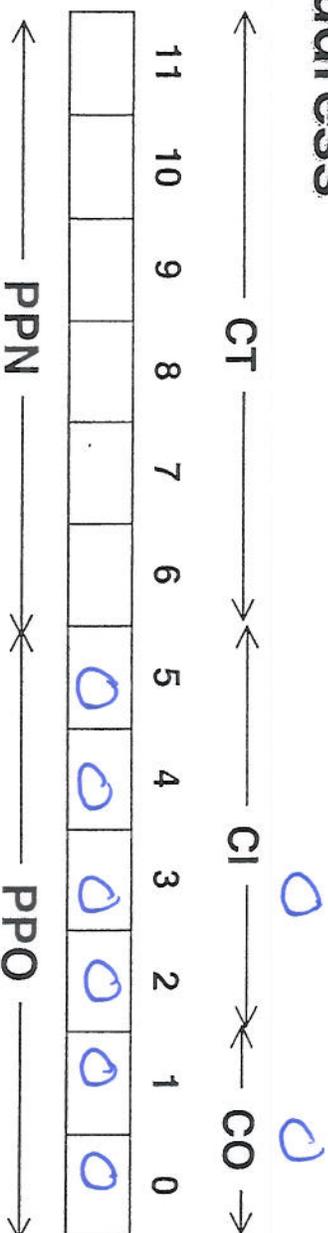
Example #3

Virtual Address 0x0040

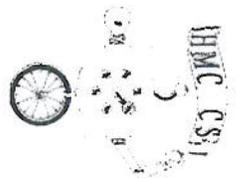


VPN 01 TLBI 1 TLBT 0 TLB Hit? N Page Fault? YES PPN: _____

Physical Address



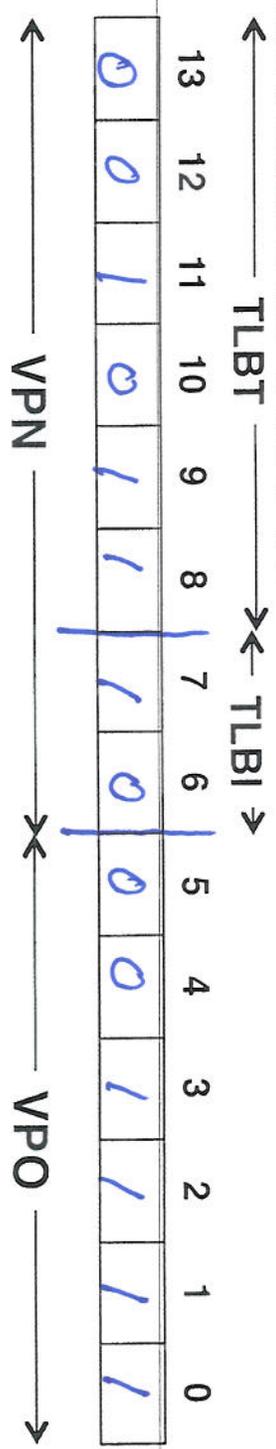
Offset 0 CI 0 CT _____ Hit? _____ Byte: _____



Address Translation

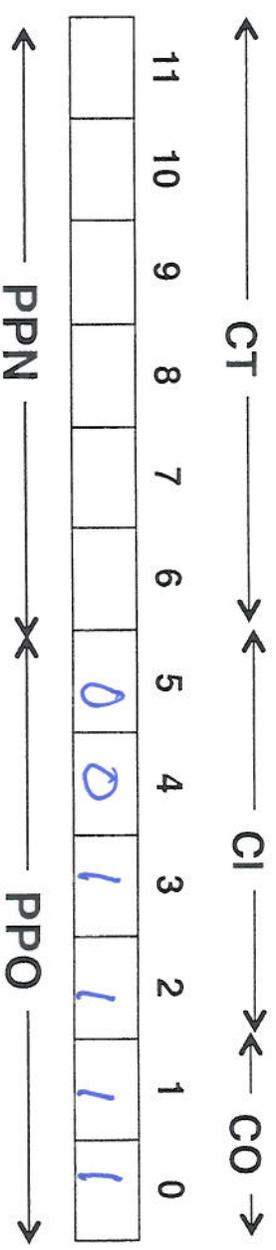
Example #2

Virtual Address 0x0B8F



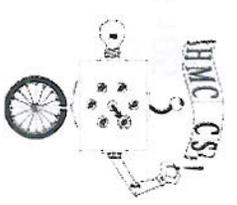
VPN 2E TLBI 2 TLBT 0B TLB Hit? N Page Fault? Y PPN: _____

Physical Address



↪ Page Table
 Target Address
 in stack
 Target as
 page miss

Offset 3 CI 3 CT _____ Hit? _____ Byte: _____

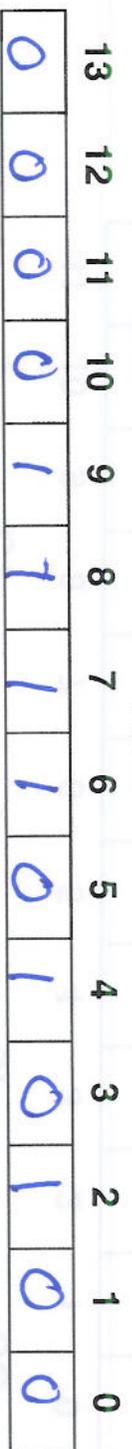


Address Translation

Example #1

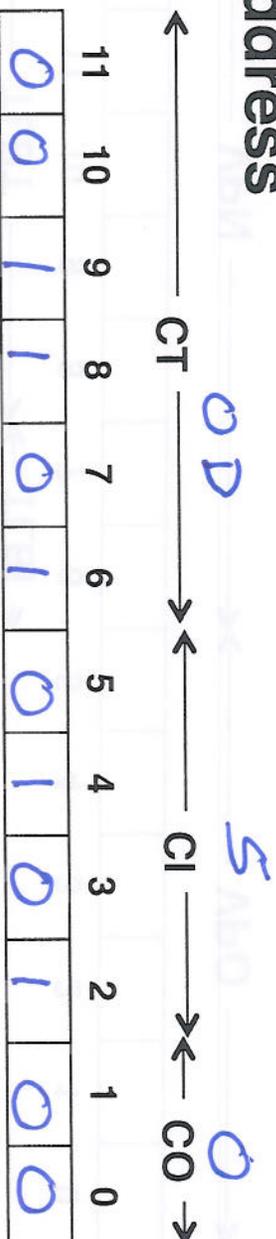
Virtual Address 0x03D4

03 ← TLBT 3



VPN 0F TLBI 3 TLBT 03 TLB Hit? Yes Page Fault? PPN: 0D

Physical Address



Offset 0 CI 5 CT 0D Hit? Yes Byte: 36

Simple Memory System Page Table



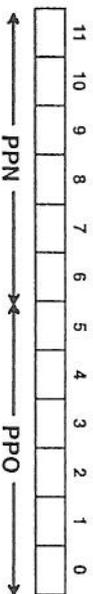
- Only shows first 16 entries

VPN	PPN	Valid	VPN	PPN	Valid
00	28	1	08	13	1
01	-	0	09	17	1
02	33	1	0A	09	1
03	02	1	0B	-	0
04	-	0	0C	-	0
05	16	1	0D	2D	1
06	-	0	0E	11	1
07	-	0	0F	0D	1

Simple Memory System Cache



- 16 lines
- 4-byte line size
- Direct mapped: CT - Tag, CI - Set/Index, CO - Byte Position



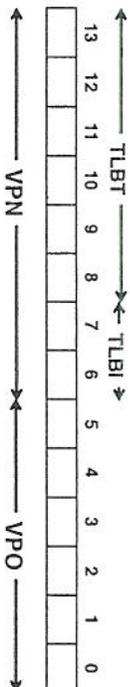
Idx	Tag	Valid	B0	B1	B2	B3	Idx	Tag	Valid	B0	B1	B2	B3
0	19	1	99	11	23	11	8	24	1	3A	00	51	89
1	15	0	-	-	-	-	9	2D	0	-	-	-	-
2	1B	1	00	02	04	08	A	2D	1	93	15	DA	3B
3	36	0	-	-	-	-	B	0B	0	-	-	-	-
4	32	1	43	6D	8F	09	C	12	0	-	-	-	-
5	0D	1	36	72	F0	1D	D	16	1	04	96	34	15
6	31	0	-	-	-	-	E	13	1	83	77	1B	D3
7	16	1	11	C2	DF	03	F	14	0	-	-	-	-

Simple Memory System TLB



TLB

- 16 entries
- 4-way associative: bits 6 & 7 - set, bits 8..13 - Tag



Set	Tag	PPN	Valid									
0	03	-	0	09	0D	1	00	-	0	07	02	1
1	03	2D	1	02	-	0	04	-	0	0A	-	0
2	02	-	0	08	-	0	06	-	0	03	-	0
3	07	-	0	03	0D	1	0A	34	1	02	-	0

Line.....