

CHAPTER 3

ASYNCHRONOUS SINGLE LINE INTERFACES

DL11

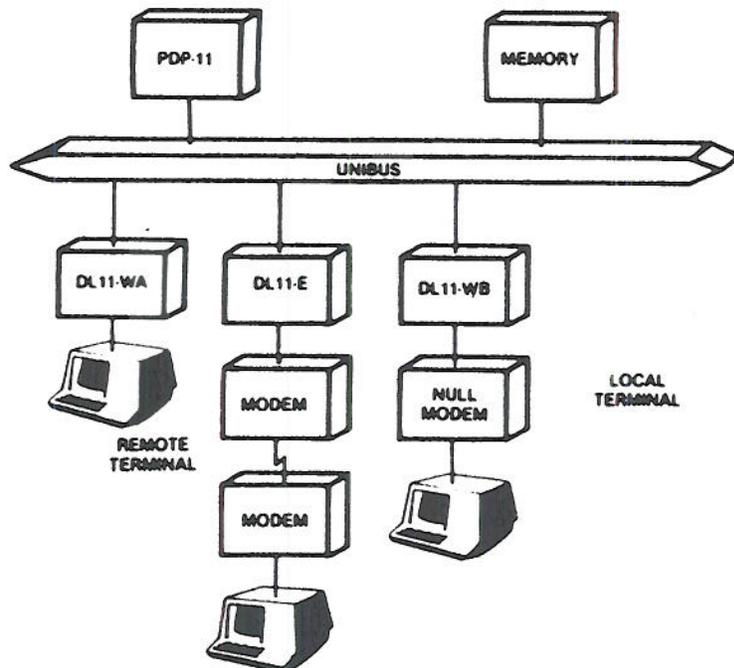
OVERVIEW/DL11

The DL11 series of asynchronous single line interfaces handles full- or half-duplex communication between a wide variety of serial communication channels and a PDP-11 computer.

With a DL11 interface, a PDP-11 computer can communicate with a local terminal such as a console DECwriter, with a remote terminal via modems and private line or public switched telephone facilities, or with another local or remote PDP-11 computer.

DL11 systems provide wide flexibility. The user can specify the data rate from a selection of standard rates between 40 and 9600 bits per second. The interface can offer split-speed operation for faster, more efficient handling of computer output.

For additional flexibility, character size, parity checking (even, odd, or none), and stop code length (1, 1.5, or 2 bits) are switch or strap selectable.



FEATURES

Double-character-buffered receiver and transmitter.

Speeds from 40 to 9600 bits per second.

Strap-selectable character size (5, 6, 7, or 8 bits), parity generation on transmit and checking on receive (even, odd, or none), stop length 1, 1.5, or 2 bits.

Standard interfacing.

Full modem control on DL11-E option.

BENEFITS

Allows a full character time for interrupt service.

Can handle a variety of terminals and communication lines at varying data rates.

Offers the ability to handle a wide range of terminals.

EIA RS-232-C/CCITT V.24, 20mA active current loop electrical interface available.

Gives the user capability of selecting full- or half-duplex operation over switched or unswitched communication lines.

PRODUCT PROFILE

General Description

Each DL11 module represents one unit to the UNIBUS and plugs into a standard small-peripheral controller slot in a PDP-11 system.

There are three DL11 models: the DL11-WA, DL11-WB, and DL11-E.

Model DL11-WB is a serial line EIA/CCITT interface and real-time line frequency clock. It is capable of handling either local or remote terminals (data only). With local devices, this model requires a null modem; in private line communication, modems are required. Switches allow modification to replace DL11-B and DL11-D in most applications. The DL11-WB gives the same wide range of operating parameters as the DL11-WA.

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Model DL11-E meets the EIA and CCITT interface specifications cited for Models B and D. This interface provides the user with the full range of data rates as well as with complete modem control for remote communication with either a terminal or another PDP-11 computer.

Model DL11-WA is a serial line 20mA interface and real-time line frequency clock. It provides the flexibility of a wide choice of speeds, character size, and stop bit configurations. Switches allow modification to replace the DL11-A and DL11-C in most applications.

OPERATION

General

The DL11 is a interface between a single asynchronous serial communication channel and the PDP-11. It performs serial-to-parallel and parallel-to-serial conversion of serial start/stop data with a double-character-buffered circuit called a UART (for Universal Asynchronous Receiver/Transmitter). This 40-pin dual-in-line package includes all of the circuitry necessary to double-buffer characters in and out, serialize/deserialize data, provide selection of character length and stop code configuration, and present status information about the unit and each character.

Receiver

The receiver section performs serial to parallel conversion of 5-, 6-, 7- or 8-level codes. The character length is selectable by split-lug jumpers on the DL11-E and by switches on the DL11-WA and DL11-WB, and is specified by the customer at the time of the order. Each character appears right-justified in the receiver data buffer register (RBUF), stripped of start, stop, and parity bits.

ASCII
OR
?
.

The data rate may lie anywhere in the range between 40 bits per second and 10,000 bits per second, and in many cases need not necessarily be the same for the receiver as for the transmitter. The receiver samples the line at 16 times the data rate.

A complete character is formed in the UART and is transferred to the receiver data buffer register (RBUF) at the time the center of the first stop bit is sampled. At that time, the Receiver Done bit (bit 7) is set in the receiver status register (RCSR). If the Receiver Interrupt Enable bit (bit 6) is also set in RCSR, an interrupt request is generated. The BR level is set by jumper plug. BR4 is standard.

The program then reads the RBUF. The character appears right-justified in bits 7-0 of RBUF, stripped of start, stop and parity (if odd or even is selected) bits. Unused high order bits (6 and 7 in the case of a

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6-level code) are zero-filled. Bits 8-11 are always zero and bits 12-15 contain status information about the character supplied by the UART.

Transmitter

The transmitter section performs parallel-to-serial conversion of data supplied to it from the UNIBUS. The character length and stop code (number of units of mark at the end of each character) are the same as for the receiver section. The transmitter section is also fully double buffered. Any time the Transmitter Ready bit (bit 7) is set in the transmitter status register (XCSR), the program may load the low-order eight bits of the transmitted data buffer register (XBUF) with a right-justified data character. The Transmitter Ready bit will be set any time the XBUF is available, whether or not a character is currently being transmitted. This is a natural result of the double buffering and means that if a character is not currently being transmitted and XBUF is empty, the program may provide two characters in succession (within less than one character time) to the transmitter.

PROGRAMMING**General**

The interface between a program running in the PDP-11 processor and DL11 is via four device registers. They are: 1) receiver status register (RCSR); 2) receiver data buffer register (RBUF); 3) transmitter status register (XCSR); and 4) transmitter data buffer register (XBUF). Each register is assigned an 18-bit memory address, and may be read from or written into using any processor instruction that references these addresses, with the exceptions noted.

Interrupts

The DL11 has two channels of interrupts: one for the receiver section (vector = XX0) and one for the transmitter section (vector = XX4). These two circuits operate independently, except that receiver takes priority on simultaneous interrupt requests (is closer to the processor on the bus).

However, it is very important to note that in the DL11-E (modem operation), the receiver section handles a multiple source interrupt: RCVR DONE and DST INT. Furthermore, DST INT is set by several conditions (RING, CARRIER, etc.). If while servicing an interrupt for one condition, a second interrupt condition occurs, a unique second interrupt (and all subsequent ones as well) may not occur. To prevent this 1) all possible interrupt conditions should be checked after servicing one particular condition, or 2) both Interrupt Enables (bits 5 and 6) should

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be cleared upon entry to the service routine for vector XXO, and set again at the end of service.

Address and Vector Assignments

The DL11-WA and DL11-WB follow the same address and vector assignments as the DL11-A and DL11-B.

SPECIFICATIONS

Function:	Provides an interface between the PDP-11 UNIBUS and a single asynchronous bit-serial communications channel.
Mechanical:	The DL11 consists of one Quad module and a connecting cable terminated in a plug appropriate to the data communications equipment to be connected.
Operating Mode:	Full- or half-duplex under program control.
Data Format:	<p>Asynchronous, serial by bit. One start and 1, 1.5 (5-level codes only), or 2 stop bits, supplied by the hardware. The DL11-WA, WB, and E will accommodate characters of 5, 6, 7 or 8 bits, with or without even or odd parity. The data format must be the same for transmitted and received data. The data format must be specified at the time of order.</p> <p>A one (1) presented by the program to any bit in the transmitted data register will cause a Marking (logical 1) condition to appear on the Transmitted Data lead during the corresponding bit interval. A zero (0) presented by the program will cause a Spacing (logical 0) condition to appear. A Marking condition on the Received Data lead during any data bit sampling interval will be presented to the program as a one (1) in the received data register, and a Spacing condition will be presented as a zero (0).</p>
Order of Bit Transmission:	Low order bit first.

DL1**Distortion:**

The DL11 receiver will operate properly in the presence of 40% space-to-mark or mark-to-space distortion between any two received data bits, and up to $\pm 4.5\%$ long-term speed distortion, provided the data format contains at least one and one-half stop units. If the data format contains only one stop unit, the speed tolerance is $\pm 4\%$. The DL11 transmitter operates with less than 3% bit-to-bit or long term distortion.

Bus Loading:

One DL11 presents one unit load to the PDP-11 UNIBUS.

Standard Interface:

The DL11-WB provides a voltage level interface and connector whose signal levels and connector pinning conform to EIA Standard RS-232-C and CCITT Recommendation V.24. The leads supported are:

	Pin	Circuit	
		EIA RS-232-C	CCITT V.24
Protective Ground	1	AA	101
Signal Ground Transmitted	7	AB	102
Data	2	BA	103
Received Data	3	BB	104
Data Terminal Ready	20	CD	108.2
Request to Send	4	CA	105

The DL11-WB is supplied with a 25-ft., 25-conductor cable terminated in a cinch DB25P plug with a protective hood.

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The DL11-E provides a voltage level interface as described above for the DL11-WB but in addition supports the following leads, giving full modem control capability to the computer program:

Data Terminal Ready, Circuit CD, pin 20.

Clear to Send, Circuit CB, pin 5.

Request to Send, Circuit CA, pin 4.

Received Line Signal Detector (Carrier), Circuit CF, pin 8.

Ring Indicator, Circuit DE, pin 22.

Secondary Transmitted Data, Circuit SBA, pin 11.**

Secondary Received Data, Circuit SBB, pin 12.**

The DL11-E is supplied with a 25-foot, 25-conductor cable terminated in a cinch DB25P plug with protective hood.

DL11-WA provides a 20mA active current loop for both Send and Receive leads for connection to local teleprinters.

The DL11-WA is supplied with a 2¼-foot, 6-conductor cable terminated with a female Mate-n-Lok connector.

* These leads are held ON (logical 1) by the hardware.

** Note that the pin assignment of these two leads conforms to that of the Bell 202 Data Set, rather than to the cited EIA/CCITT standard.

Power Requirements:

The DL11 requires 1.8 amps of +5V, 0.05 amps of +15V, and .15 amps of -15V.

DL11-WA, WB

2.0 amps at +5V

0.05 amps at +15V

0.15 amps at -15V

DL11-E

1.8 amps at +5V

0.05 amps at +15V

0.15 amps at -15V

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Data Rate:

The DL11-E is supplied to customer order with 13 standard data rates in four groups:

Group 1: 110 bits per second receive and transmit.

Group 2: 134.5 bits per second receive and transmit.

Group 3: Following 8 speeds, which may be different for receive and transmit: 50, 75, 150, 300, 600, 1200, 1800, 2400 bits per second.

Group 4: Following 8 speeds, which may be different for receive and transmit: 200, 300, 600, 1200, 2400, 4800, 7200, 9600 bits per second.

The DL11-WA, WB is supplied with eight switch-selectable speeds: 110, 150, 300, 600, 1200, 2400, 4800, 9600 bits per second.

ORDERING INFORMATION

DL11-WB

Single asynchronous serial line EIA/CCITT interface and real-time line frequency clock.

DL11-E

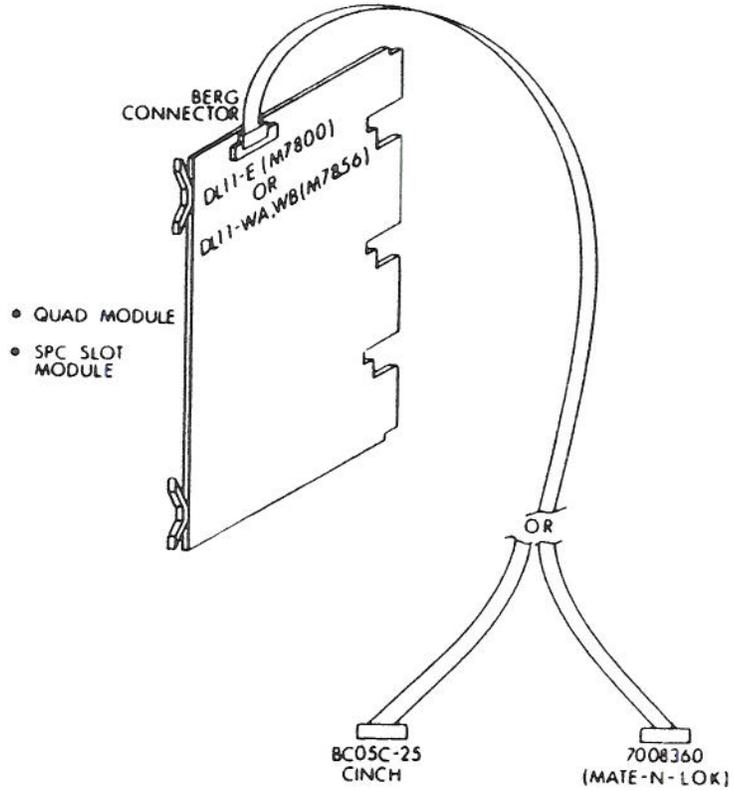
Single asynchronous serial line interface. Supports full modem control interface, including Data Terminal Ready, Clear to Send, Request to Send, Carrier, Ring, Secondary Received and Secondary Transmitted leads.

DL11-WA

Single asynchronous serial line 20mA interface and real-time line frequency clock.

Asynchronous Single Line Interfaces

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DL11 SINGLE LINE ASYNCHRONOUS INTERFACE

NOTE

See Programming section for register information.